Journal of Engineering and Applied Science Vol. 07, No. 01, pp. 09–15, December 2023

Journal of Engineering and Applied Science

Contents are available at www.jeas.ruet.ac.bd

Design and Analysis of Tunnel Field Effect Transistor for Low Power Application

Labib Yeamen[1], Sunjidah Hossain[2], Md. Faruk Hossain[3]

[1,2,3]*Department of Electrical & Electronic Engineering, Rajshahi University of Engineering & Technology, Bangladesh*

ARTICLE INFORMATION

Received date: 27th Oct 2023
Revised date: 17th Dec 2023
Accepted date: 31st Dec 2023

Keywords

Band to Band Tunnelling
Subthreshold Swing
Double Gate

ABSTRACT

Tunnel Field Effect Transistor is a semiconductor device designed for low power consumption which utilizes band to band tunnelling as a carrier injection mechanism. The objective is to integrate a minimal leakage current to enhance the energy efficiency of the Tunnel Field Effect Transistor relative to a MOSFET. An optimized model of Double Gate Tunnel Field Effect Transistor has been developed that can be utilized in low power applications. Increasing emergence of the Internet of Things (IoT) have led to a need for devices that operate at low supply voltage and exhibit low leakage behaviour. The proposed model has lower leakage current, higher I_{on}-I_{off} ratio and steeper Subthreshold Swing than previous research work. It has been shown by varying the channel length, material, source and drain doping concentration. The subthreshold swing found to be 11.91 mV/decade, and obtained I_{on}/I_{off} ratio is 4.60724×10^{9} which ensures that this model is a possible contender for low power application.

1. Introduction

Major problems, including gate tunnel current, coupling and parasitic effects, as well as short channel effects, such as drain induced barrier lowering, high leakage current, subthreshold swing and lower ON to OFF current ratio have arisen as a result of the scaling of MOSFETs in recent years. Due to these facts, power consumption is much in case of a conventional MOSFET. Tunnel Field Effect Transistor (TFET) has emerged as a possible alternative of MOSFET. It uses Band to Band Tunnelling as a carrier injection mechanism to achieve a lower subthreshold swing below 60 mV/decade. To make the TFET more energy efficient than a MOSFET, low leakage current and low SS are combined. The rise of mobile applications and the Internet of Things (IoT), which contain a plethora of always on sensor nodes, has increased the demand for devices with low supply voltage (V_{DD}) and low-leakage operation [1–2]. By utilizing the quantum mechanical process of tunnelling, a TFET seeks to meet this demand and overcome the demerits of MOSFET. TFET ensures the following advantages:

- Steeper subthreshold swing.
- Lower leakage Current.
- Higher Ion/Ioff ratio.
- Improved threshold voltage.

For these benefits, Tunnel Field Effect Transistors have attracted substantial research attention recently. Tripathy et al [3] achieved I_{on}/I_{off} ratio of 2.4×10^{8} with a steep subthreshold slope by using Si-Ge Pocket JL-TFET. Using Charge Plasma DL-DG TFET, Ion/Ioff ratio was found $5x10^{8}$ [4]. Trapezoidal Channel Double Gate TFET provided a subthreshold swing of 23mV/decade [5]. Singh et al [6] got a subthreshold swing of 53.7mV/decade using his proposed model. NC GaAs/InN TFET exhibited a SS of 19.2mV/decade and an improved I_{on}/I_{off} ratio [7]. An optimized TFET model

* Corresponding authors: Department of Electrical & Electronic Engineering, Rajshahi University of Engineering & Technology, Bangladesh
E-mail addresses: engr.mfhossain@ruet.ac.bd (Dr. Md. Faruk Hossain)

has been proposed here which will ensure both lower subthreshold swing and higher I_{on}/I_{off} ratio than the previous works. This model can be used in various low power applications instead of a MOSFET.

2. Proposed Device Structure

An optimized TFET model is designed in this work which has double gate symmetrically on both side for boosting the on current. This structure provides an improved control over electric field in the channel which ensures precisely controlled tunnelling barrier. The dual gate helps to tune the width and height of the tunnelling barrier. Tunnelling probability is exponentially sensitive to these barrier parameters. This control over the barrier will minimize the off current. In this way, it will maximize the on-state current. High ratio of on current and off current is necessary for a better performance and this structure of double gate tunnel field effect transistor will contribute on this.

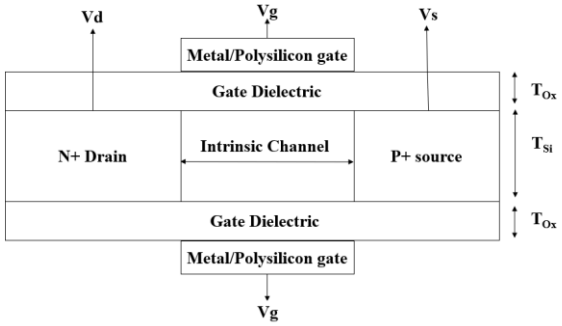

Figure 1. Cross Sectional View of Double Gate Tunnel Field Effect Transistor

The parameters used for this model is shown in Table 1.

Table 1. Simulation Parameter used in Proposed Model

Device Parameter	Symbol	Used Values
Source Doping	N_{source}	1×10^{22}atom/cm^3
Drain Doping	N_{drain}	5×10^{18}atom/cm^3
Channel Doping	N_{ch}	1×10^{18}atom/cm^3
Source Length	L_{source}	50 nm
Drain Length	L_{drain}	50 nm
Channel Length	L_{ch}	20 nm
Gate oxide thickness	t_{ox}	3 nm
Gate work function	Φ_m	4.5 eV

All these parameters have been achieved by varying different device parameters such as channel material, channel length, doping concentrations on TCAD device simulator tool where the model was developed. This model has a unique double gate design which makes possible to control electron tunnelling efficiently. For designing the device model, the following methodology was followed.

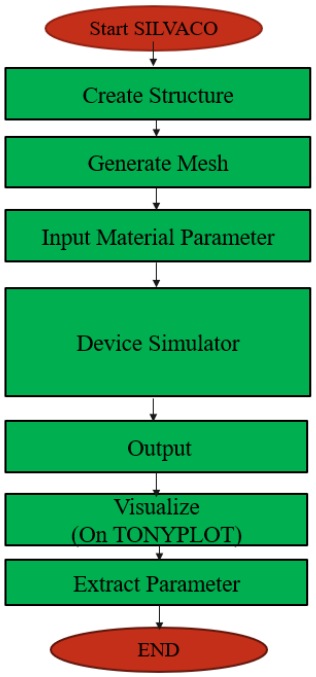

Figure 2. Simulation Methodology on SILVACO

3. Impact of Device Parameter

There are some certain impacts of device parameter like channel length, channel material, source and drain doping concentration on DGTFET model.

3.1 Channel Material

TFETs use quantum tunnelling principle to transfer charge carriers through a barrier. Channel material in TFET is important for optimizing the performance. The impact of the channel material on TFETs can be significant in various factors of their operation, including the tunnelling probability, carrier mobility, thermal stability and overall device characteristics. Table 2 shows the comparison of subthreshold swing and I_{on}-I_{off} ratio for different channel length.

Table 2. Different value of SS, I_{on}, I_{off}, Ratio of I_{on} & I_{off} in different channel material

Channel Material	SS (mV/dec.)	I_{ON} (A)	I_{OFF} (A)	I_{ON}/I_{OFF}
InGaAs	143.6	9.770×10^{-5}	1.0626×10^{-7}	919.442
MoS_2	42.83	2.168×10^{-8}	3.6765×10^{-17}	5.89751×10^{8}
CdS	59.60	2.528×10^{-10}	4.2667×10^{-16}	592624
GaAs	16.30	1.027×10^{-6}	1.9323×10^{-15}	5.31731×10^{8}

This comparison is also analysed on TCAD device simulator.

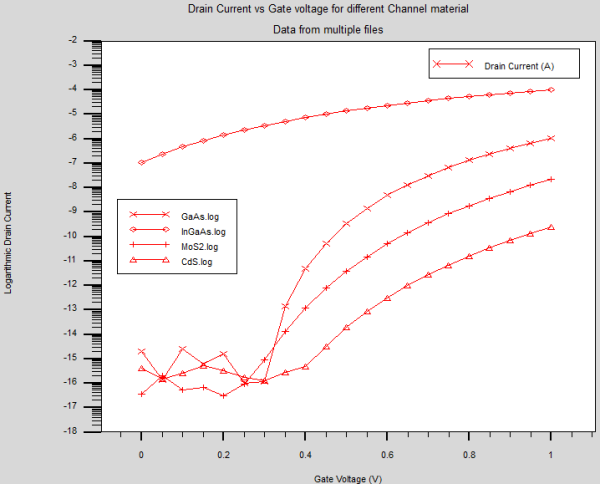

Figure 3. Logarithmic I_d Vs Vg Curve for different channel material

Among these channel materials, GaAs has relatively narrow bandgap, higher electron mobility and thermal stability which not only allows faster charge carrier transportation within the channel but also increases reliability in various operating condition. So, due to these electrical properties and effectivity, GaAs was selected as channel material for the DGTFET model.

3.2 Channel length

In contrast to a conventional MOSFET, the drain current in a TFET shows little dependence on the channel length [8-10]. The channel length has a direct impact on the threshold voltage of the TFET. TFETs are recognized for having steeper subthreshold swing. A lower SS and threshold voltage is typically the result of a shorter channel length. A TFET can operate with low power consumption and quicker switching due to a shorter channel length. Higher on state currents are typically made possible by smaller channel lengths because they enable more effective electron tunnelling over the barrier separating the source and drain regions. So, TFET operation is greatly influenced by channel length in terms of all these factors. Table 3 shows the comparison of subthreshold swing and I_{on}-I_{off} ratio for different channel length.

Table 3. Different value of SS, I_{on}, I_{off}, Ratio of I_{on} & I_{off} in different channel length

CHANNEL LENGTH	SS (MV/ DEC.)	I_{ON} (A)	I_{OFF} (A)	I_{ON} / I_{OFF}
20 nm	11.91	9.175×10^{-7}	1.9914×10^{-16}	4.60724×10^{9}
30 nm	37.80	9.4234×10^{-7}	6.7735×10^{-16}	1.3912×10^{9}

From Table 3 it's evident that channel length has an impact on TFET. This comparison was observed on the simulator as well.

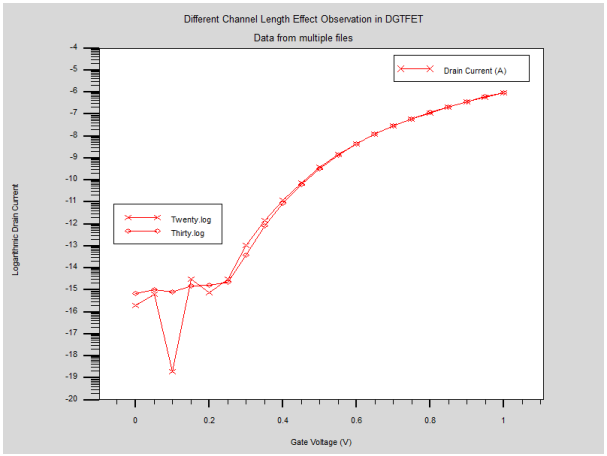

Figure 4. Logarithmic I_d Vs Vg Curve for different channel length

As a result, 20 nm channel length was selected for the optimized model.

3.3 Source Doping Concentration

When the source doping concentration is increased, the bandgap narrowing increases, which results in a decrease in the tunnelling distance [11-12]. Hence tunnelling probability increases and on state current improves. Experimental results show that doubling the source doping concentration leads to two times increase in the I_{on} of a TFET [11]. For high source doping concentration, due to the modified built-in potential at the source channel junction, the threshold voltage is expected to reduce [11]. As a result, TFET will turn on more easily and will achieve faster switching with better performance. Higher source doping concentration may result in better subthreshold swing as well that will enhance the possibility for low power consumption. The comparison of subthreshold swing and I_{on}-I_{off} ratio for various source doping concentration is presented on Table 4.

Table 4. Different value of SS, I_{on}, I_{off}, Ratio of I_{on} & I_{off} in different source doping concentration

DOP. CONC.	CURVE TITLE	SS (mV/ dec.)	I_{ON} (A)	I_{OFF} (A)	I_{ON}/ I_{OFF}
1×10^{17}	S1	60.59	4.2×10^{-4}	6.81×10^{-12}	6.1×10^{7}
1×10^{19}	S2	50.77	2.97×10^{-15}	5.23×10^{-15}	1.76
1×10^{20}	S3	27.78	5.80×10^{-8}	1.79×10^{-16}	3.237×10^{8}
1×10^{22}	S4	11.91	9.175×10^{-7}	1.99×10^{-16}	4.61×10^{9}

In the comparison curve below, the S4 curve indicates better outcome in case of SS and I_{on}/I_{off}.

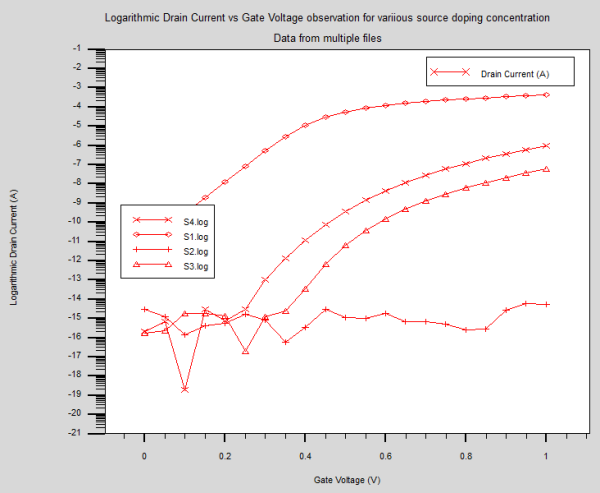

Figure 5. Logarithmic I_d Vs Vg Curve for various source doping concentration

At a lower source doping concentration, the model showed an unusual behaviour. Lower doping concentration in the source region limits the number of charge carrier injection in the channel which reduces the current drive capability. Moreover, it escalates the source resistance which leads to an increased parasitic effect. On the contrary, the increasing concentration helps in optimizing the performance of the model to a certain level. Higher source doping concentration can be achieved through ion implantation or diffusion process. Electron Beam Lithography (EBL) plays a crucial part in these processes by defining the region where doping is to occur. It involves creating a pattern on semiconductor substrate. Techniques like RTA can be used after implantation to enhance the dopant activation and thus achieve a higher doping concentration in the source region. For an improved performance, source doping concentration of 1×10^{22} atom/cm^3 was selected for the proposed model.

3.4 Drain Doping Concentration

When the drain doping concentration is increased, tunnelling probability increases and on state current improves. But it may eventually cause increase in the off-state current too as highly doped drain gives opportunity for the electron to tunnel through the barrier even in the off-state condition. So, trade off might be necessary in case of value selection of the concentration. For high drain doping concentration, the threshold voltage is expected to reduce. As a result, TFET will turn on easily and will achieve faster switching. Table 5 indicates the comparison of subthreshold swing and I_{on}/I_{off} ratio for different drain doping concentration.

Table 5. Different value of SS, I_{on}, I_{off}, Ratio of I_{on} & I_{off} in different drain doping concentration

DOP. CONC.	CURVE TITLE	SS (mV/ dec.)	I_{ON} (A)	I_{OFF} (A)	I_{ON}/I_{OFF}
5×10^{16}	D1	32.17	9.11×10^{-7}	3.486×10^{-17}	2.6151×10^{10}
5×10^{17}	D2	20.30	9.125×10^{-7}	4.973×10^{-18}	1.835×10^{11}
5×10^{18}	D3	11.91	9.175×10^{-7}	1.991×10^{-16}	4.6072×10^{9}

Table 5 shows better outcome in case of SS and Ion/Ioff by using drain doping concentration of 5×10^{17} atom/cm^3 & 5×10^{18} atom/cm^3 respectively.

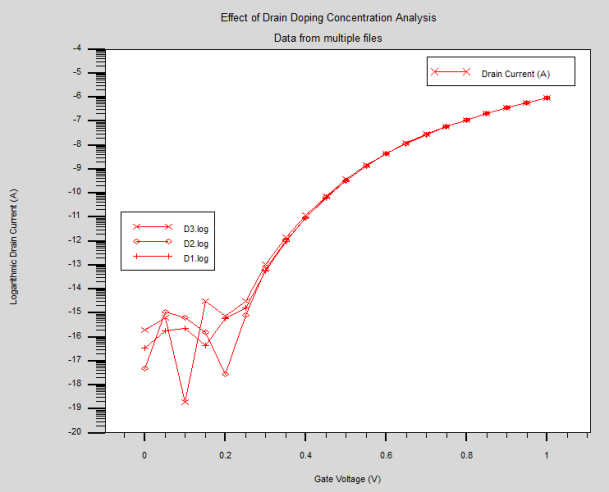

Figure 6. Logarithmic I_d Vs Vg Curve for various drain doping concentration

Figure 6 also indicates, For D2 curve, the value of I_{on}/I_{off} ratio is better. But for D3 curve, subthreshold swing is better. By keeping in mind to have both lower subthreshold swing and higher I_{on}/I_{off} ratio, trade-off is necessary. Due to this, 5×10^{18} atom/cm^3 is used as drain doping concentration in the proposed model.

4. Result & Discussion

After performing vast analysis on various device parameters such as channel material, channel length, doping profiles, an optimized model is designed using SILVACO. Proposed DGTFET model is shown below.

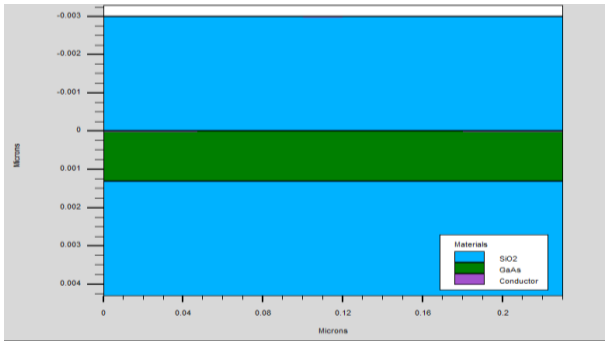

Figure 7. 2D Structure of proposed DGTFET Model

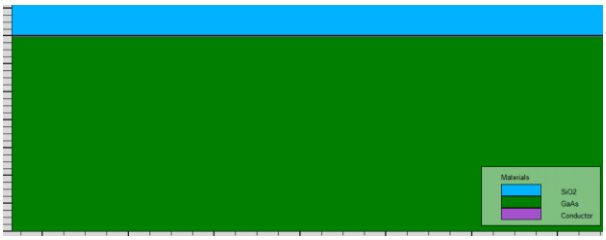

Figure 8. Different layer observation of the DGTFET Model

Band to Band Tunnelling phenomenon of the proposed model was observed in Figure here. With sufficient Gate bias, it occurs in intrinsic region. Conduction band aligns with valance band. Electrons in valance band of p region tunnels with intrinsic region of conduction band. Hence current flows in device. But when gate bias reduces, bands misalign and no current flows. This helps greatly in low power application.

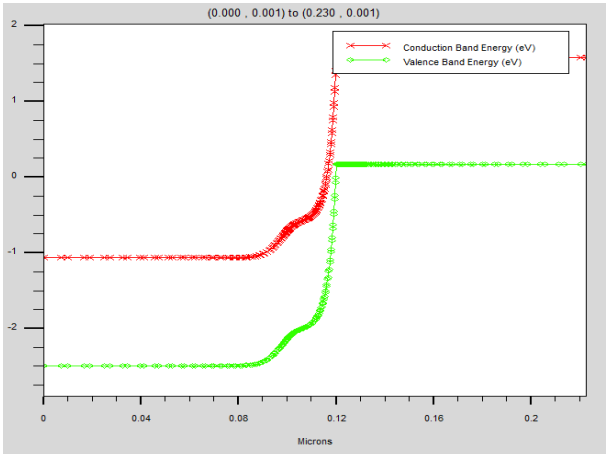

Figure 9. Band to Band Tunnelling observation in the energy band diagram of the proposed DGTFET model

After following proper algorithm and running the code, various parameters were extracted. Subthreshold Swing (SS) is one of them. It is achieved by following equation.

$$SS = \frac{\Delta Vgs}{\Delta(\log Id)} \qquad (1)$$

Moreover, transfer characteristics of the model was found on TONYPLOT of the TCAD simulator.

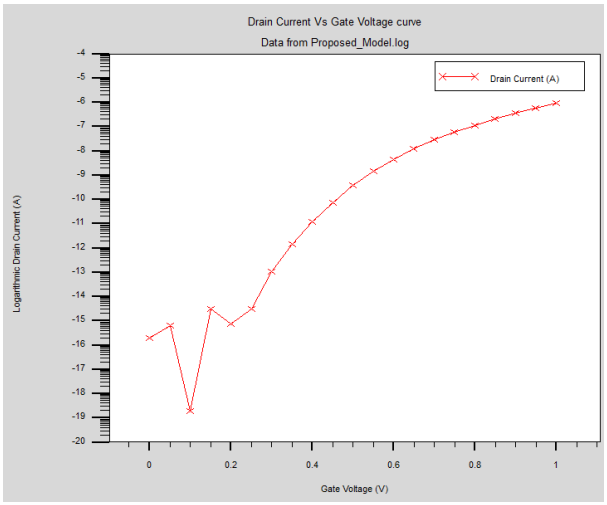

Figure 10. Logarithmic I_d Vs Vg Curve of proposed DGTFET

The subthreshold swing is observed steeper in Figure 10 for the proposed model.

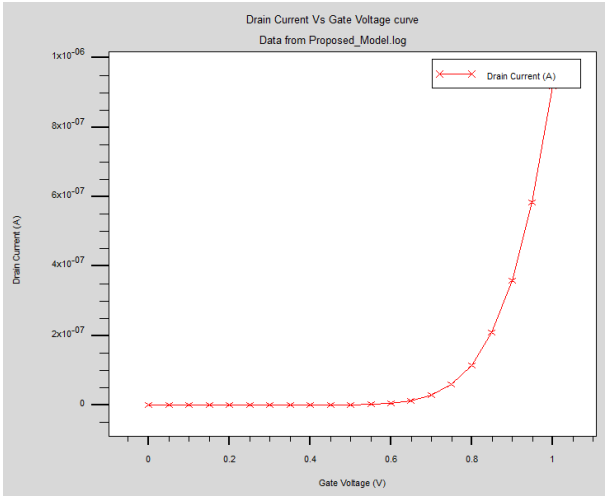

Figure 11. I_d Vs Vg Curve of proposed DGTFET

The threshold voltage is seen to be 0.7V in Figure 11. Both the figure represents steeper subthreshold swing and improved threshold voltage respectively which results in improved on current to off current ratio. It makes this model to be energy efficient. But the presence of dual gate may increase the probability of gate tunnelling leakage. Even a non-ideality factor like interface trap can affect the tunnelling behaviour and device performance.

This proposed structure has been compared with different research work to be validated for using in low power application.

Table 6 shows the comparison of extracted values of this optimized model with the values extracted by various researchers in recent years.

Table 6. Comparison of extracted values from proposed model with recent works

REF NO.	DEV. SPEC.	SS (mV/ dec)	I_{ON} (A)	I_{OFF} (A)	I_{ON}/ I_{OFF}
(S. Sinha *et al.*,2021) [13]	Ge source-based L TFET	21	2.12×10^{-5}	1.09×10^{-13}	2×10^{9}
(H.W. Kim *et al.*,2021) [14]	Si TFET	26	10^{-7}	10^{-16}	10^{9}
(D. Keighobadi *et al.*,2021) [15]	InGaAs /InP TFET	27	0.5×10^{-6}	5×10^{-12}	10^{5}
(A. Walia *et al.*,2021) [16]	Dual Metal TFET	37.81	72.82×10^{-6}	0.131×10^{-9}	5.517×10^{5}
(K. Tamersit *et al.*,2022) [17]	EDJL-CN TFET	43	1.34×10^{-6}	1.23×10^{-11}	10^{5}
(K. Mondol *et al.*,2022) [18]	DG TFET	33.9	-	-	1.41×10^{9}
(S. Howldar *et al.*,2023) [19]	Hetero dielectric TFET	-	1.34×10^{-5}	7.83×10^{-11}	1.711×10^{5}
(A. Zirak *et al.*,2023) [20]	JL TFET	40	4.4×10^{-5}	10^{-11}	4.4×10^{6}
Proposed Work	**Double Gate TFET**	**11.91**	**9.175×10^{-7}**	**$1.991 43\times 10^{-16}$**	**4.6072×10^{9}**

Finally, by going through all these comparisons, even though having a little non ideality issue it is proved evidently that our proposed model is better in terms of lowering leakage current, subthreshold swing and achieving better threshold voltage. This proposed model of DGTFET has both steeper SS and higher Ion/Ioff ratio which makes it more efficient in low power application.

5. Conclusion

In this work, we have developed a simulation-based model of DGTFET. For a TFET, the subthreshold swing and Ion/Ioff ratio both are paramount parameters as they are major concern for low power application. The model was developed after analysing impact of various channel length, channel material, doping profile. GaAs was used as the channel material of the model where channel length was 20 nm, source doping concentration was 1×10^{22}atom/cm^3 and drain doping concentration was 5×10^{18}atom/cm^3. The subthreshold swing found to be only 11.91 mV/decade, and obtained I_{on}/I_{off} ratio is 4.60724×10^{9}. The value of subthreshold swing (SS) and Ion/Ioff ratio was then compared with some recent works of researchers which validates our DGTFET model. The proposed model can be applied to various low power application like Bio-Sensing Application, Energy Harvesting Systems, Environmental Monitoring Nodes, Green Energy Systems, Implantable Medical Devices, IoT Sensors, Portable Environmental Sensors, Ultra Low Power Radio Receivers, Wearable Health Monitors, Wireless Sensor Networks, etc. Our proposed model will provide standard performance in low power systems and high-speed devices in this era of modern technology.

References

[1] R. Aitken, V. Chandra, J. Myers, B. Sandhu, L. Shifren, and G. Yeric, "Device and technology implications of the internet of things," in *VLSI Technology (VLSI-Technology): Digest of Technical Papers, 2014 Symposium on*, pp. 1–4, IEEE, 2014.

[2] W. Dehaene and A. Verhulst, "New devices for internet of things: A circuit level perspective," in *Electron Devices Meeting (IEDM), 2015 IEEE International*, pp. 25.5.1–25.5.4, Dec 2015.

[3] S. Tripathi and G. S. Patel, "Design of low power Si0.7Ge0.3 pocket junction-less tunnel FET using below 5 nm technology," *Wireless Personal Communications*, vol. 11, no. 4, pp. 2167–2176, Jan. 2020.

[4] Mishra, V., Verma, Y. K., Agarwal, L., & Gupta and S. K., "Temperature impact on device characteristics of charge plasma-based tunnel FET with Si0.5Ge0.5 source," *Engineering Research Express*, 2021.

[5] B. Goswami, P. Das, and A. Roy, "Trapezoidal Channel Double Gate Tunnel FET Suitable for Better Scalability, Speed and Low Power Application," *Devices for Integrated Circuit*, pp. 532-544, Jan. 2021.

[6] A. Singh, S. K. Sinha, and S. Chander, "Impact of Fe Material Thickness on Performance of Raised Source Overlapped Negative Capacitance Tunnel Field Effect Transistor (NCTFET)," *Silicon*, vol. 14, pp. 9083–9090, 2022.

[7] A. A. M. Mazumder, K. Hosen, M. S. Islam and J. Park, "Numerical Investigations of Nanowire Gate-All-Around Negative Capacitance GaAs/InN Tunnel FET," in *IEEE Access*, vol. 10, pp. 30323-30334, 2022.

[8] C. Sandow, J. Knoch, C. Urban, Q.-T. Zhao, and S. Mantl, "Impact of electrostatics and doping concentration on the performance of silicon tunnel field-effect transistors," *Solid-State Electronics*, vol. 53, pp. 1126–1129, Oct. 2009.

[9] K. Boucart and A. M. Ionescu, "Length scaling of the double gate tunnel FET with a high-k gate dielectric," *Solid-State Electronics*, vol. 51, pp. 1500–1507, Nov. 2007.

[10] S. Saurabh and M. J. Kumar, "Impact of strain on drain current and threshold voltage of nanoscale double gate tunnel field effect transistor: Theoretical investigation and analysis," *Japanese Journal of Applied Physics*, vol. 48, June 2009.

[11] (accessed October 21, 2023) Tunnel field-effect transistor [Online]. Available: https://en.wikipedia.org/wiki/Tunnel_field-effect_transistor

[12] (accessed October 22, 2023) Lower power Consumption in TFET vs MOSFET [online]. Available: https://phys.org/news/2012-11-compact-tunnel-field-effect-transistors.html

[13] S. Sinha and R. Chaudhary, "Ge-Source Based L-Shaped Tunnel Field Effect Transistor for Low Power Switching Application," *Silicon*, vol. 14, pp. 7435-7448, Oct. 2021.

[14] H. W. Kim and D. Kwon, "Steep Switching Characteristics of L-Shaped Tunnel FET With Doping Engineering", *IEEE Journal of the Electron Devices Society*, vol. 9, pp. 359-364, 2021.

[15] D. Keighobadi, S. Mohammadi, and M. Mohtaram, "Switching Performance Investigation of a Gate-All-Around Core-Source InGaAs/InP TFET," *Transactions on Electrical and Electronic Materials*, vol. 22, pp. 502–508, 2021.

[16] Walia, Akshit; Kaushal, Priya; and Khanna, Gargi. "Impact of Temperature on the Performance of Tunnel Field Effect Transistor," 2021.

[17] K. Tamersit, A. Kouzou, H. Bourouba, R. Kennel, and M. Abdelrahem, "Synergy of Electrostatic and Chemical Doping to Improve the Performance of Junction-less Carbon Nanotube Tunnelling Field-Effect Transistors: Ultra-scaling, Energy-Efficiency, and High Switching Performance," *Nanomaterials*, vol. 12, p. 462, 2022.

[18] K. Mondol, M. Hasan, A. H. Siddique, and S. Islam, "Quantization, gate dielectric, and channel length effect in double-gate tunnel field-effect transistor," *Results in Physics*, vol. 34, p. 105312, 2022.

[19] S. Howldar, B. Balaji, and K. Srinivasa Rao, "Design and Qualitative Analysis of Hetero Dielectric Tunnel Field Effect Transistor Device," *International Journal of Engineering, Transactions C: Aspects*, vol. 36, no. 06, pp. 1129–1135, 2023.

[20] A. Zirak, "Improvements in reliability and radio frequency performance of junction-less tunnelling field effect transistor using p pocket and metal strip," *IET Circuits, Devices & Systems*, vol. 17, 2023.